WHAT IS CLAIMED IS:

1. A method for depositing a silicon carbide layer onto a substrate, the method comprising steps of providing a silicon source, carbon source and nitrogen source and an inert gas into a reaction zone, the reaction zone containing the substrate; producing an electric field in the reaction zone, the electric field generated using low and high frequency RF energy produced by an RF power supply, the RF power supply generating an average power at an electrode surface used for plasma discharge in the reaction zone; and reacting the silicon and carbon source gas to deposit a silicon carbide film on the substrate; wherein the RF power supply generates high frequency RF power and low frequency RF power during a processing period.

2. The method of Claim 1, wherein:

the high frequency RF power has a frequency between about 13 MHz and about 30 MHz, and has a power between about 200 watts and about 1000 watts; and

the low frequency RF power has a frequency between about 100 kHz and about 500 kHz, and has a power between about 50 watts and 500 watts.

3. The method of Claim 1, wherein a ratio of the low frequency RF power to a total RF power is less than about 0.5.

4. The method of Claim 1, wherein the average power at the electrode surface is substantially constant.

5. The method of Claim 1, wherein the silicon and carbon source gas is one of the following: tri-methylsilane, tetra-methylsilane, or divinyl-dimethylsilane.

6. The method of Claim 1, wherein the inert gas is one of the following: helium, argon or krypton.

7. A method of Claim 1, wherein the nitrogen source in either one of the following or both: Ammonia (NH3) or Nitrogen (N2).

8. The method of Claim 1, wherein the ratio of the silicon and carbon source gas to the inert gas is between about 1:1 and about 1:15.

9. The method of Claim 1, wherein the silicon and carbon source gas is provided into the reaction zone at a rate between about 200 sccm and about 500 sccm.

10. The method of Claim 1, wherein the substrate is heated to a temperature between about 200 °C and about 400 °C.

11. The method of Claim 13, wherein the substrate is heated to a temperature between about 320 °C and about 350 °C.

12. The method of Claim 1, wherein the reaction zone is maintained at a pressure between about 300 Pa and about 1000 Pa.

13. The method of Claim 15, wherein the reaction zone is maintained at a pressure between about 500 Pa and about 700 Pa.

14. The method of Claim 1, wherein the silicon carbide layer is nitrogen-doped, and wherein the nitrogen-doped silicon carbide layer has a dielectric constant less than about 5.0.

15. The method of Claim 1, wherein the silicon carbide layer has a compressive film stress.

16. The method of Claim 15, wherein the silicon carbide layer has a leakage current of less than $1x10^{-8}$A/cm2 at an electric field of 1MV/cm.

17. The method according to Claim 1, wherein the film is an etch stop layer.

18. The method according to Claim 1, wherein the film is a hard mask.

19. A method for manufacturing on a semiconductor substrate an interlayer structure containing a film in contact with a copper layer, comprising the steps of:

(i) forming multiple layers on a semiconductor substrate;

(ii) forming a hole for an interlayer connection of the multiple layers by etching;

(iii) depositing copper in the hole;

(iv) removing an excess of the copper from a top of the multiple layers;

(v) depositing a silicon carbide film on the top of the multiple layers by plasma reaction, wherein the copper is covered by the silicon carbide film.

20. The method according to Claim 19, wherein the multiple layers comprise a lower etch stop layer, a lower low dielectric layer, an intermediate etch stop layer, an upper low dielectric layer, and in step (ii) an upper etch stop layer laminated in sequence on the substrate, and the hole is produced by forming a resist on top of the upper etch stop layer and

forming a via hole and trench by etching the multiple layers using the resist, and in step (iv) the resist and the upper etch stop layer are removed when removing the excess of the copper.

21. The method according to Claim 19, wherein prior to step (i), a low dielectric layer is formed on the substrate, and the multiple layers are formed on top of the low dielectric layer.

22. The method according to Claim 19, wherein steps (i) through (iv) are repeated at least once.